C 6072   (Pages : 2)   Name.............................

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2010

EC 04 404 – COMPUTER ORGANIZATION AND ARCHITECTURE

(2004 Admissions)

Time : Three Hours   Maximum : 100 Marks

I. (a) Define the terms : (i) Microprogramming ; (ii) Multiprogramming.

    (b) What are the different types of instructions ?

    (c) Define hardwired control.

    (d) List the rules for floating point addition and subtraction.

    (e) Compute the hit ratio for a virtual memory system having MS access time of 500 n sec, secondary access time of 20 m sec. and average access time of 4.4 m sec. Describe the suitable hardware/software schemes to reduce the average access time below 2.5 m sec.

    (f) Describe the principle of generating the CRC code for an IO data block.

    (g) Describe relative advantages/disadvantages of various bus arbitration schemes.

    (h) Explain Flynn's classification of various computer organizations.

$$(8 \times 5 = 40 \text{ marks})$$

II. (a) (i) Explain the basic functional units of a computer with neat block diagram.

      (ii) Give the control sequence for executing the single word instruction ADD (R0), (R1), (R2) where the first two are the source operands and the third is the destination operand for a single bus organization.

$$(10 + 5 = 15 \text{ marks})$$

Or

    (b) (i) Explain the difference between two operand and three operand instruction formats.

      (ii) What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor registers ?

$$(8 + 7 = 15 \text{ marks})$$

III. (a) (i) Explain the microprogrammed control unit organization and classification of micro instruction.

      (ii) Explain the difference between hardwired control and microprogrammed control.

$$(10 + 5 = 15 \text{ marks})$$

Or

Turn over

    (b)   Design an accumulator based CPU control unit with following instructions :

           (i)   Data transfer ; (ii) Data processing.

                                                                           (15 marks)

IV.   (a)   (i)   Write the carry expression for five stage carry look ahead adder.

              (ii)   Illustrate in detail about non-restoring division algorithm for unsigned integer with example.

                                                       (5 + 10 = 15 marks)

<center>*Or*</center>

    (b)   (i)   Define ALU. What are the various operations performed in ALU ?

             (ii)   Show the contents of registers E, A, Q and SC during the process of division of (i) 1010001100 by 101110 (ii) 100011110 by 101100.

                                                       (8 + 7 = 15 marks)

V.   (a)   (i)   Define Cache memory. Explain all types of mapping processes followed in cache memory.

             (ii)   What is meant by memory interleaving? Show the distribution of addresses for a memory system consisting of two banks of four 1 K memory modules to form an 8 K memory system. Give the main memory address format.

                                                     (10 + 5 = 15 marks)

<center>*Or*</center>

    (b)   (i)   Define peripherals. What is parallel processing ?

             (ii)   Clearly specify the sequence of actions associated with the following modes of data transfer :

                      (1)   Synchronous.

                      (2)   Asynchronous with one-way and two-way control.

                                                        (5 + 10 = 15 marks)

                                                            [4 × 15 = 60 marks]