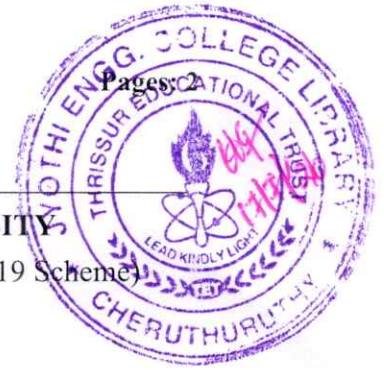


Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP/S2PT) Examinations May 2026 (2019 Scheme)



Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Convert hexadecimal 8A9D ₁₆ to binary and decimal	3
2	Convert -46 and 25 to binary and add using the 2's complement form.	3
3	Using boolean algebra techniques, simplify the expression $A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C$	3
4	Use a K-Map to simplify the expression $DE\bar{F} + \bar{D}E\bar{F} + \bar{D}\bar{E}\bar{F}$ to a minimum SOP form.	3
5	Draw and explain the combinational circuit for a half subtractor circuit.	3
6	Implement the function $F(A,B,C,D) = \sum(0,2,4,5,8,9)$ with a multiplexer.	3
7	What are the functions of preset and clear inputs for a flip flop	3
8	What is a Parallel IN- Serial Out register.	3
9	Compare PAL, PLA and ROM .	3
10	Draw the schematic diagram of R-2R ladder type DAC	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

- | | | |
|-------|--|----|
| 11 | Explain an Error detection and correction code using a suitable example. | 14 |
| 12 a) | Draw and Explain the schematic diagram of TTL NAND gate. | 7 |
| b) | Convert 45600 ₈ to binary and 7765 ₈ to decimal. | 7 |

Module -2

- | | | |
|----|---|----|
| 13 | Using K-Map map method obtain the minimum sum of the products and minimal product of sums expression for the function
$F(A,B,C,D) = \sum(0,2,3,6,7) + d(8,10,11,15)$ | 14 |
|----|---|----|

- 14 a * Design a full adder circuit and implement it using two half adders. 14
b What are the advantages of carry look ahead adder over parallel adder? explain

Module -3

- 15 a) Construct a 4 to 16 lines decoder using 3 to 8 lines decoder. 7
b) Explain the architecture of Arithmetic Logic Unit. 7
16 Explain the steps to design a BCD to seven segment decoder with multiplexers. 14

Module -4

- 17 a) Design a MOD-10 ripple counter using T flip flop and draw the timing diagram 10
b) Draw the logic circuit of D flip flop using T flip-flop 4
18 a) Design a synchronous counter using J-K Flip flop to count the sequence 14
0,1,3,5,7,0,1,3.....

Module -5

- 19 a) What are the important specifications of a D/A converter 7
b) Explain flash type A/D converter with diagram. 7
20 a) Explain the characteristics of a Mealy machine. 7
b) Implement the basic AND and OR gates using Verilog 7
