Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP/S2PT) Examinations May 2026 (2019 Scheme)

Course Code: ECT206
Course Name: COMPUTER ARCHITECTURE AND MICROCONTROLLERS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Describe the roles of the program counter (PC), and stack pointer (SP) in processor operation.	3
2	Represent −25 and +19 in 1's complement, and 2's complement (use 8 bits).	3
3	Explain why Port 0 behaves differently from Ports 1 to 3.	3
4	Explain how 8051 interrupts are enabled and prioritized.	3
5	Write an 8051 C program to send values 00 to FF to port P1 with a delay in between the values.	3
6	Explain how key bounce impacts keyboard interfacing and how it is handled.	3
7	Describe the purpose of R13 (SP), R14 (LR), R15 (PC) and CPSR in the ARM7 register set.	3
8	Explain the functions of any three bits in SCON.	3
9	Differentiate programmed I/O and interrupt driven I/O.	3
10	Discuss the concept of DMA and its importance in computer systems.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Use shift and add multiplication algorithm to compute $(-13) \times (+11)$. Write the steps, draw the flowchart of the algorithm and show the final binary and decimal result.	9
	b)	Illustrate Von Neumann vs Harvard using block diagrams, then tabulate the main benefits and limitations.	5
12	a)	Perform the binary division of $7 \div -3$ using division algorithm. Show the step-by-step results and include a flowchart of the algorithm.	9
	b)	Describe the importance of the opcode fetch and decode stages in executing an	5

instruction.

Module -2

13 a) For each instruction, name the addressing mode and show how the effective address/data is obtained: 6

(i) MOV A, #3CH (iii) MOV A, @R0 (v) MOVC A, @A+DPTR

(ii) MOV A, 30H (iv) MOV @R1, A (vi) SJMP NEXT.

b) Describe the classes of 8051 instructions—data transfer, arithmetic, logical, and branch—and give two examples of each with their instruction length (bytes) and typical machine cycles. 8

14 a) Write an 8051-assembly routine to copy 16 bytes from internal RAM 40H–4FH to 60H–6FH. 8

b) Compare a microcontroller with a general-purpose microprocessor. Give an embedded applications where the 8051 is a good fit and justify. 6

Module -3

15 a) Design an 8051-assembly program for interfacing LEDs connected to Port 1 such that a "running light" (where LEDs turn ON one after another in sequence so that it looks like the "light is moving") pattern moves from P1.0 to P1.7 and then repeats continuously with a visible delay between shifts. Assume on-board crystal of 12 MHz. 8

b) With the help of a neat diagram, explain the steps involved in interfacing a common-anode 7-segment display with the 8051 using a port. Discuss how segment codes are generated. 6

16 a) An 8051 is used to drive a unipolar stepper motor through a driver circuit connected to Port 0. Write a C code for the sequence of coil excitation required for full-step clockwise rotation. 8

b) Distinguish between software delay using instruction loops and hardware delay using timers in 8051. Comment on the advantages and disadvantages of both methods. 6

Module -4

17 a) Distinguish between timer mode and counter mode of the 8051. How is the mode selected? 7

b) Write an 8051 C program to receive characters serially at 9600 baud and echo them back to the sender. 7

18	a)	Define assembler, compiler, linker, and loader. Explain the role of each tool in the program development cycle, highlighting the difference between assembling, compiling, linking and loading.	7
	b)	Explain how to configure TMOD and TCON for using Timer 0 as an event counter to count the number of pulses arriving at pin T0 (P3.4) in one second assuming a 12 MHz crystal.	7

Module -5

19	a)	Explain the direct mapping of Cache memory with an example.	7
	b)	Explain the working of DRAM and SRAM with neat diagram.	7
20	a)	Explain address translation in virtual memory.	7
	b)	Explain associative mapping of cache memory for a 16K cache with block size 256 and word size 32. Draw the necessary figures. Specify the main memory address format.	7

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