Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP/S2PT) Examinations May 2026 (2019 Scheme)

Course Code: CST202
Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A
(Answer all questions; each question carries 3 marks)

		Marks
1	Illustrate how the effective address is calculated in the indexed and base indexed addressing mode with suitable examples.	(3)
2	In a single bus organisation, list the registers which are connected to both the external and internal buses. Which are the signals associated with these registers?	(3)
3	Show the design of a logic circuit and its function table which implements the four logic operations OR, XOR, AND, NOT.	(3)
4	Show the logical left shift and logical right shift operations on bit pattern 11100111.	(3)
5	Consider a 4 stage linear instruction pipeline processor and an equivalent non-pipelined processor for executing 4 instructions I1,I2,I3 and I4. Calculate the speed up of this 4 stage linear instruction pipeline processor over the non pipelined processor with necessary equations.	(3)
6	Design a 2x2 array multiplier and label it.	(3)
7	Differentiate between the horizontal and vertical organization of microinstructions in terms of its organisation, speed and storage requirement.	(3)
8	A processor is being designed for a safety critical application where the response time is very crucial. Which type of control unit is suitable for this situation? Why?	(3)
9	Illustrate how the fast page mode improves the access speed in DRAMs.	(3)
10	How many bits are in the tag, line and offset fields, if the main memory is 24 bit addressable and Cache memory is 64K bytes with 16 byte cache blocks.	(3)

PART B
(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Explain three address, two address and one address instructions, giving examples	(9)

for each. Evaluate (A*B) + (C/D) and store result in SUM using three address, two address and One address format with relevant assumptions

b) Write the control sequence for the execution of the instruction: DIV R1, (R2) (5)

12 a) What is the importance of addressing modes in computer architecture? Explain any 4 types of addressing modes with an example for each. (10)

b) What is Byte addressability? Differentiate between Big endian and Little-endian assignment of memory with necessary diagrams. (4)

Module -2

13 a) Show the design a 4-bit Arithmetic unit for performing the basic arithmetic operations of addition and subtraction. Give the function table also. (7)

b) What is the purpose of using status registers? Name and explain the use of any FOUR status bits in status register. Show the hardware design for setting these bits in the status register. (7)

14 a) Design a 4-bit combinational logic shifter with 2 control signals H1 and H2 that perform the following operations (bit values given in parenthesis are the values of control variable H1 and H2 respectively.): Transfer of 0's (00), shift right (01), shift left (10), no shift (11). (9)

b) Draw and explain the organization of a processor unit employing a scratchpad memory. (5)

Module -3

15 a) Illustrate the hardware arrangement for performing restoring integer division. Use this algorithm to compute the quotient and remainder when the **dividend is 15** and the **divisor is 3.** (10)

b) Explain Write After Read (WAR) and Read After Write (RAW) hazards with proper examples. (4)

16 a) Explain the concept of an arithmetic pipeline. Illustrate how floating point addition can be performed using arithmetic pipelines. (9)

b) Name the algorithm that can be used effectively for both signed and unsigned multiplication. Also explain the steps of the algorithm. (5)

Module -4

17 a) Describe the components and working of a microprogrammed control unit with suitable diagram. Summarize the advantages and disadvantages of a microprogrammed control unit over hardwired control unit. (10)

b) Illustrate PLA control logic with suitable diagram. (4)

18 Illustrate the steps for the design of a hardwired control unit using one flip-flop per state method to implement the addition and subtraction of two fixed-point binary numbers represented in sign-magnitude form. (14)

Module -5

19 a) Illustrate any two ways by which a processor can handle two or more simultaneous interrupt requests from multiple devices? (7)

b) Explain how DMA is employed in I/O organization to enhance data transfer between peripheral devices and memory? Differentiate between cycle stealing DMA and burst mode DMA. (7)

20 a) Illustrate the Direct, Associative and Set Associative cache memory mapping schemes with necessary diagrams/ examples. (9)

b) Explain the working of Content Addressable Memory (CAM). (5)

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