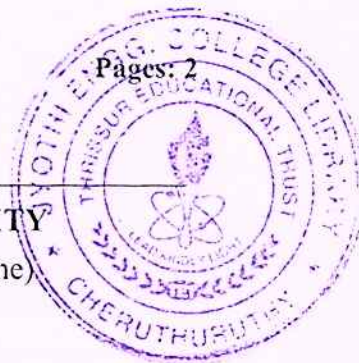




Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
B.Tech Degree S3 (S,FE) Examinations June 2026 (2019 Scheme)

Course Code: RAT205

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Define Fan-out of a logic family.	3
2	Represent 1987_{10} . (a) in Octal (b) in BCD (c) in Excess three code.	3
3	Explain the reason why Ex-OR gate is known as controlled inverter.	3
4	Define propagation delay(t_{PD}) of a logic gate.	3
5	Describe Race-around condition in level triggered JK-FF.	3
6	Describe how we can use D-FF to count up the input clock pulses.	3
7	Define the relationship between the no. of FFs and no. of counting states of a Ring counter and a Johnson counter.	3
8	List different types of shift registers.	3
9	Represent the basic Module syntax of Verilog HDL.	3
10	List the different types of RAM.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

- | | | |
|----|---|----|
| 11 | a) Explain in detail about the digital logic family characteristics. | 10 |
| | b) Differentiate binary weighted and non-weighted codes with example. | 4 |
| 12 | a) Generate a table of binary codes and Gray codes of numbers from 0 to 15. | 6 |
| | b) Draw the internal circuit of CMOS NAND gate circuit and explain. | 8 |

Module -2

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|----|---|----|
| 13 | a) Implement Full adder using 3x8 decoder. | 10 |
| | b) Differentiate between MUX and Decoder. | 4 |
| 14 | a) Explain the working of three bit Carry Look ahead adder with the help of diagram. | 8 |
| | b) Obtain a minimal sum of products expression for the function
$F(A, B, C, D) = \sum m(1, 8, 9, 10, 12, 14, 15) + \sum d(0, 2, 3, 4)$ | 6 |

Module -3

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|----|----|---|---|
| 15 | a) | Convert a D Flipflop to a T Flipflop. | 7 |
| | b) | Explain the working of a JK Flipflop with necessary diagrams, state and excitation table. | 7 |
| 16 | a) | Explain with diagram the working of a master slave JK Flipflop. | 6 |
| | b) | Design a mod-9 asynchronous counter with state diagram and timing diagram. | 8 |

Module -4

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|----|----|--|----|
| 17 | a) | Explain the working of a 4-bit Ring counter with the help of a circuit diagram. | 8 |
| | b) | Describe with diagram the working of a 4-bit parallel in serial out (PISO) Shift Register. | 6 |
| 18 | a) | Design a Mod 10 binary synchronous counter using T flip flop. | 14 |

Module -5

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|----|----|---|---|
| 19 | a) | Explain the read and write operations of a basic DRAM cell with necessary diagrams. | 7 |
| | b) | Write Verilog Code for a 2x1MUX circuit. | 7 |
| 20 | a) | Explain the difference between PLA and PAL with necessary diagrams. | 7 |
| | b) | Implement Full adder using PLA | 7 |
