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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) (FT/WP/S1PT) Examinations May/June 2026 (2019 Scheme)

Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	Convert 302.62510 to binary and hexadecimal.	(3)
2	Differentiate between Verilog and C++.	(3)
3	Show that the dual of XOR operation is also its complement.	(3)
4	Write the verilog code to implement the following boolean function using structural method. F(A,B,C) = AB + BC	(3)
5	Implement a 4 – bit parallel adder.	(3)
6	Write the verilog code for a half adder.	(3)
7	Differentiate flip flops from latches	(3)
8	Implement a JK flip flop using a D flip flop.	(3)
9	Define fan out and noise margin.	(3)
10	Explain the operation on a CMOS invertor.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11.a	Use 2's complement method to find 6510 – 7810. Represent the result as both binary and decimal numbers.	(8)
11.b	Explain the types of operators in Verilog with examples.	(6)
12.a	Represent the DCBA16 as (i) BCD, (ii) Gray code, (iii) Excess 3 code	(6)
12.b	Explain fixed and floating point representation of numbers with examplesd	(8)

Module 2

13	Consider the Boolean function F = Σ(0, 2, 5, 7, 8, 10, 13,15) (i) Obtain Canonical SOP expression (ii) Minimise the expression using K-Map (iii) Express the minimised expression in terms of NAND operations only. (iv) Write Verilog code for the minimised expression	(14)

14 Consider the Boolean function F = Π(1,3,4,6,9,11,12,14) (14)
(i) Obtain Canonical POS expression
(ii) Minimise the expression using K-Map
(iii) Express the minimised expression in terms of NOR operations only.
(iv) Write Verilog code for the minimised expression

Module 3

15.a Implement the logic function f(A,B,C,D)=∑m(0,2,3,5,9,12,15) using (8)
(i) 16:1 MUX (ii) 8:1 MUX

15.b Write the verilog code for a 8:1 MUX (6)

16.a Design a 4 bit Gray code to binary converter circuit. (8)

16.b Write a verilog code to implement the circuit designed in 16.a (6)

Module 4

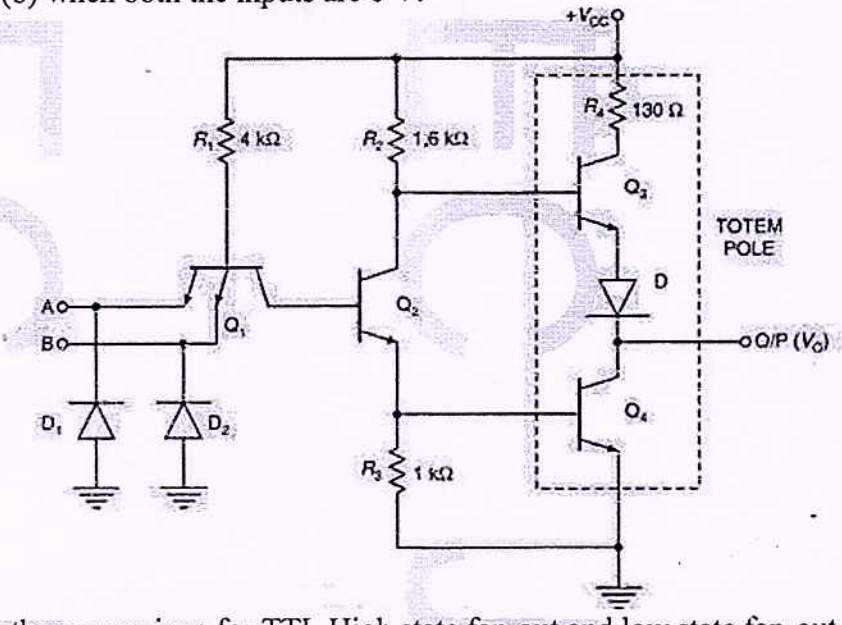
17 Design a sequence generator circuit using T flip flops to generate the following sequence : 0 – 1 – 3 – 4 – 2 – 5 – 7 – 6 – 0 (14)

18.a Explain the operation of a 4-bit Johnson counter with circuit diagram, truth table and waveforms. (8)

18.b Explain about race around condition with relevant waveform. Explain how this condition is solved. (6)

Module 5

19.a In the following figure, the 7400 NAND gate has *V*CC = +5 V and a 5-kΩ load connected to its output. Find the output voltage (a) when both the inputs are + 5 V and (b) when both the inputs are 0 V. (10)



19. b Write the expressions for TTL High state fan-out and low state fan-out. Also, mention what is the actual fanout capability of the gate. (4)

20.a Draw the symbols and switching action of NMOS and PMOS. (4)

20.b Explain CMOS NAND gate with circuit diagram, equivalent circuits for various inputs and truth table. (10)

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