Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) (FT/WP/S1PT) Examinations May/June 2026 (2019 Scheme)

Course Code: CST203
Course Name: Logic System Design

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 Add the following numbers using a) 1's complement method b) 2's complement method. (3)

-(82)+34.

2 Find even and odd parity bit of the following binary numbers. (3)

a) 10111

b) 11111

3 Find Standard SOP and POS forms of the expression AB+ABC+A (3)

4 Differentiate Tabulation method and K-map simplification method. (3)

5 Design Half adder using NAND gate. (3)

6 Draw the circuit diagram of 1:4 Demultiplexer. (3)

7 Explain Sequential and combinational circuits. (3)

8 Differentiate latches and flipflops. (3)

9 How to represent (85.125) in Single precision floating point. (3)

10 Give algorithm for BCD addition. (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 a) Represent the numbers +100 and -100 in Signed magnitude, 1's complement and 2's complement representations. (4)

b) Explain Hamming Code. (4)

c) Convert $(1000111)_2$ into base 8, 10 and 16. (6)

12 a) Find BCD and Excess-3 code for the decimal numbers 198 and 213. (4)

b) Add, subtract, multiply and divide the following binary numbers. (8)

10001 and 00110

And verify the answer by using decimal arithmetic.

c) Explain any 2 Character Coding Schemes. (2)

Module 2

13 Simplify the following functions using Kmap.

a) $f(A,B,C,D,E)=\sum m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)$ (6)

b) $f(A,B,C,D)=\sum(0,1,8,9,10)+d(2,4,6)$ (4)

c) $f(A,B,C)=\prod(1,2,3)$ (4)

14 a) Solve X+XY by using Boolean algebra laws. (2)

b) State and prove Demorgans law. (4)

c) Design all logic gates NOT, AND, OR and XOR using universal gates NAND and NOR. (8)

Module 3

15 a) Design 8:3 encoder and 3:8 decoder circuit. (7)

b) Implement BCD adder. (7)

16 a) Design 4 bit parallel adder by using full adders. (7)

b) What are the advantages of Carry look ahead adder and design the circuit. (7)

Module 4

17 a) Design 4 bit up/down synchronous and asynchronous counters. (14)

18 a) Differentiate different triggering. (4)

b) What do you mean by race around condition? Explain how to avoid. (6)

c) Give some applications of fliflops and counters. (4)

Module 5

19 a) Describe the working of Programmable Logic Array (PLA) with suitable example. (7)

b) Design 4 bit Johnson and Ring counters. (7)

20 a) Explain the working of 4 bit shift registers. (8)

b) Give algorithm for the following. (6)

1. 2's complement adder/subtractor.
2. Floating point addition.

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