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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R,S) / S4 (WP) (R) / S2 (PT) (S, FE) Examination May 2024 (2019 Scheme)

Course Code: EET 206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1 Perform the following number conversions. (3)

a) $(875.84)_{10}$ to hexadecimal b) Gray code 110010 to binary.

2 What is meant by a universal gate? List two universal gates and write its truth table. (3)

3 Prove that $AB + \bar{A}C = (A + C)(\bar{A} + B)$, where A, B, and C are logic variables. (3)

4 State De Morgan's theorem. Simplify the Boolean expression $f(P,Q) = \overline{\overline{PQ} + \bar{P} + PQ}$ into minimum number of literals by applying De Morgan's theorem. (3)

5 What is the advantage of a priority encoder over an encoder? (3)

6 Draw the block diagram of a 4:1 multiplexer. Write down its function table and develop a Boolean expression for its output. (3)

7 What are the asynchronous inputs to a flip-flop? Explain its function. (3)

8 Compare the functioning of S-R flip-flop and J-K flip-flop with the help of truth tables. (3)

9 Differentiate between Moore and Mealy state machines. (3)

10 What is FPGA? What are the components of a typical FPGA logic block? (3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11 a) Express $(-81.75)_{10}$ in binary using (i) 12-bit 2's complement form, and (ii) sign-magnitude form. (6)

b) Explain the working of TTL NAND gate with the help of an internal diagram. (8)

12 a) Determine the range of 4 bit binary number which is expressed in (i) signed magnitude form (ii) 1's complement form (iii) 2's complement form. (6)

b) Explain the working of CMOS NOR gate with the help of an internal diagram. (8)

Module -2

13 a) Expand the Boolean function, $f(A,B,C) = A\bar{B}C + \bar{C} + \bar{A}C$ into canonical SOP form. (4)

b) Derive an expression for the sum and the carry of a full adder. Implement the derived sum and carry expressions using only NAND gates. (10)

14 a) Implement the Boolean function $f(X,Y,Z) = \sum m(1,2,3,4,5,7)$ using minimum number of NAND gates. (4)

b) What is a carry look-ahead adder? Why is it preferred over parallel adders? Draw the logic circuit of a full adder which can generate look-ahead carry bit. (10)

Module -3

15 Explain the working of a comparator which can compare two 2-bit binary numbers, $A = A_2A_1$ and $B = B_2B_1$ (A_1 *and* B_1 are the LSB and A_2 and B_2 are MSB). Deduce expressions for the outputs when $A > B$, $A < B$, and $A = B$. Implement these expressions using logic gates. (14)

16 a) Implement the following sum of minterms expression using an 8:1 multiplexer. $f(A,B,C,D) = \sum m(0,2,5,7,12,13,14,15)$. (7)

b) What is the significance of parity bit? Draw the logic circuit diagrams of an even parity bit generator and checker for a 4-bit data. (7)

Module -4

17 a) Draw the logic diagram of a 4-bit Johnson counter which employs D flip-flops. Write down its count sequence table and draw the timing diagram. (10)

b) What is a shift register? List down any three applications of shift registers. (4)

18 Design and implement a mod-6 synchronous up-counter using J-K flip-flops. Draw the state diagram and relevant excitation table. Also, check for lock-out condition. (14)

Module -5

19 a) Write the Verilog code for AND gate, OR gate and half adder. (4)

b) With the help of a neat circuit diagram, explain how a R-2R ladder type DAC converts a digital signal to analog signal. (10)

20 a) Differentiate between PAL and PLA. (4)

b) Explain the working of a flash type analog to digital converter (ADC) with the help of a neat circuit diagram. (10)

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