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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree Examination June 2022 (2019 Scheme)

Course Code: ECT304

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1		What is FPGA? What are the characteristics and applications of FPGA	(3)
2		Compare Top down and Bottom up approach in VLSI design	(3)
3		Design a 2x1 multiplexer using CMOS logic	(3)
4		Draw the circuit of a MOS inverter with saturated NMOS load	(3)
5		What are the issues associated with NP domino logic	(3)
6		Compare DRAM and SRAM cells	(3)
7		What is the need for array multipliers	(3)
8		Mention the worst-case delay associated with Carry-Bypass adder, Linear Carry-Select adder, Square- root carry select adder	(3)
9		What is meant by lithography? Explain various types of Lithography	(3)
10		With an example, explain the role of stick diagram in VLSI design	(3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11	a)	With neat diagram explain the design flow of FPGA	(7)
	b)	What is SoC? What are the applications? Draw the internal architecture of SoC	(7)

OR

12	a)	Explain the term ASIC. Differentiate between full custom and semi custom ASIC	(10)
	b)	Explain the significance of power considerations in VLSI	(4)

Module II

13	a)	Illustrate CMOS inverter DC characteristics with neat diagrams. Explain the different regions	(10)
	b)	Implement the 4x1 multiplexer using Transmission gates	(4)

OR

14 a) What is meant by pass transistor logic? What are the differences in transmission characteristics of N MOS and P MOS transistors? (10)

b) Realize the logic function X= ((A+B).(C+D))' using CMOS logic (4)

Module III

15 a) Design three transistor and one transistor DRAM cells and explain the working of each types (10)

b) Explain the basic principle of operation of dynamic logic (4)

OR

16 a) Design a 4x4 NAND based MOS ROM Cell Array and explain its operation (10)

b) Compare the performance of dynamic and domino logic (4)

Module IV

17 a) With diagram illustrate the principle of operation of an array multiplier (4)

b) Design a 16-bit square-root carry select adder and indicate the worst-case delay (10)

OR

18 a) Design a 4X4 array multiplier. Show the critical path and also estimate the delay of the multiplier. (10)

b) Write the advantages of square-root carry select adder compared to linear carry select adder (4)

Module V

19 a) What are the steps in wafer preparation fabrication (4)

b) Describe in detail about the production of single crystalline silicon from CZ process (10)

OR

20 a) With neat diagram explain molecular beam epitaxy (8)

b) What is meant by design rules? Write short notes on various rules in VLSI chip design. (6)

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